data, correspond to the LL signal of FIG. **1**), modulate the encoded and interleaved information word bits, and map the modulated information word bits to constellation points.

[0044] In this case, the first and second encoders **111** and **121** may include an outer encoder (not shown) and an inner encoder (not shown) to encode the information word bits using a concatenated code.

[0045] Here, as an outer code performed before an inner code in the concatenated code, a Bose, Chaudhuri, Hocquenghem (BCH) code may be used, and as the inner code, a low density parity check (LDPC) code may be used.

[0046] To this end, the first and second encoders **111** and **121** may include a BCH encoder (not shown) and an LDPC encoder (not shown).

[0047] In this case, the BCH encoder (not shown) may perform BCH encoding for the information word bits to generate BCH parity bits, and the LDPC encoder (not shown) may perform LDPC encoding for a BCH codeword including the information code bits and BCH parity bits, that is, LDPC information word bits to generate LDPC parity bits.

[0048] An LDPC codeword generated by such encoding may be represented as illustrated in FIG. **2**. As illustrated in FIG. **2**, the LDPC codeword may have a form in which the BCH parity bits and the LDPC parity bits are sequentially added to the information word bits.

[0049] Meanwhile, the LDPC encoder (not shown) may encode the LDPC information word bits according to various code rates to generate the LDPC codeword having various lengths.

[0050] For example, the LDPC encoder (not shown) may encode the LDPC information word bits at the code rates of 3/15, 4/15, 5/15, 6/15, 7/15, 8/15, 9/15, 10/15, 11/15, 12/15, and 13/15 to generate the LDPC codeword having the length of 16200 or 64800.

[0051] Meanwhile, although the example described above illustrates the case in which the BCH is used as the outer code, this is merely one example, and a cyclic redundancy check (CRC) code instead of the BCH code may also be used.

[0052] In this case, the first and second encoders **111** and **121** may include a CRC encoder (not shown) and an LDPC encoder (not shown).

[0053] Specifically, the CRC encoder (not shown) may perform CRC encoding for the information word bits to generate CRC parity bits, and the LDPC encoder (not shown) may perform LDPC encoding for a CRC codeword including the information word bits and CRC parity bits, that is, LDPC information word bits to generate LDPC parity bits. The LDPC codeword generated by such encoding may have a form in which the CRC parity bits and the LDPC parity bits are sequentially added to the information word bits.

[0054] According to an exemplary embodiment, however, the first and second encoders **111** and **121** may or may not include both the BCH encoder (not shown) and the CRC encoder (not shown).

[0055] Meanwhile, the first gain controller **130** may adjust power of a signal output from the first BICM encoder **110** by multiplying a gain value $\sqrt{P_{UL}}$ with the signal output from the first BICM encoder **110**, and may adjust power of a signal output from the second BICM encoder **120** by multiplying a gain value $\sqrt{P_{LL}}$ with the signal output from the second BICM encoder **120**. In this case, $\sqrt{P_{UL}}^2+\sqrt{P_{LL2}}=1$.

[0056] In addition, the signal of which the power is adjusted by the first and second gain controllers **130** and **140** may be overlapped with each other by the adder **150**, the time interleaver **160** may interleave constellation points to which the signal output from the adder **150** is mapped, that is, cells, and the OFDM transmitter **170** may map the interleaved cells to an OFDM frame to transmit the mapped cells to the receiving apparatus **1000**.

[0057] In this case, one example of the constellation for the LDM signal may be represented as illustrated in FIG. **3**.

[0058] FIG. **3** illustrates a case in which the upper layer signal is modulated with quadrature phase shift keying (QPSK), and lower layer signal is modulated with 64-quadrature amplitude modulation (64-QAM), by way of example. As such, in the LDM signal, the constellation points for the lower layer signal having the relatively small power are overlapped with each other based on the constellation points for the upper layer signal having the relatively large power.

[0059] However, FIG. **3** describes the case in which the upper layer signal is modulated with the QPSK, and the lower layer signal is modulated with the 64-QAM, but this is merely one example. That is, the upper layer signal may be modulated with the QPSK, and the lower layer signal may also be modulated with 256-QAM.

[0060] Meanwhile, FIG. **1** describes the case in which the power for each of the signal output from the first BICM encoder **110** and the signal output from the second BICM encoder **120** is adjusted, and the signals having the adjusted power are then overlapped with each other.

[0061] However, as illustrated in FIG. **4**, power of a signal output from a second BICM encoder **120** is first adjusted, the signal having the adjusted power and a signal output from a first BICM encoder **110** are added by an adder **150**, and power of the overlapped signal may be then adjusted. In this case, a gain value of a first gain controller **130** may be $\sqrt{P_{UL}}$, and a gain value of a second gain controller **140** may be

$$\sqrt{\frac{P_{LL}}{P_{UL}}}.$$

Meanwhile, an LDPC encoding process refers to a process of generating an LDPC codeword satisfying $H \cdot C^T = 0$ for LDPC information word bits. Here, H denotes a parity check matrix, and C denotes the LDPC codeword. That is, the LDPC encoding process refers to a process of generating parity bits in which a summation obtained by multiplying respective columns of the parity check matrix with respective LDPC codeword bits becomes a '0' vector.

[0062] Accordingly, the transmitting apparatus **100** may prestore the parity check matrix using a memory (not shown), and LDPC encoders (not shown) of the first and second encoders **111** and **121** may encode the LDPC information word bits using the parity check matrix.

[0063] Meanwhile, a parity check matrix according to an exemplary embodiment may have a structure as illustrated in FIG. **5**.

[0064] The parity check matrix **10** illustrated in FIG. **5** has the same structure as the parity check matrix defined in an advanced television system committee (ATSC) 3.0 standard. Hereinafter, the parity check matrix **10** will be schematically described.